AMENDMENTS TO THE CLAIMS:

Please cancel claims 1 – 21 and 31 - 48.

Please amend claims 22 – 30 as follows:

22. (Amended) A chip scale package ~~for a semiconductor device containing a plurality of electronic circuits, said chip scale package~~ comprising:

a semiconductor body having ~~a size and shape configured to accommodate the plurality of electronic circuits in the semiconductor device~~ a top surface and a bottom surface; and

wherein no active electronic circuitry is present on the semiconductor body;

a via having a via top portion beginning at ~~a~~ said top surface of said semiconductor body and extending through ~~said die~~ to a via bottom portion on ~~a~~ said bottom surface of said semiconductor body;

an input/output (I/O) interconnect physically and electrically coupled to said via bottom portion, said I/O interconnect structure being located within an area on the bottom surface of said die; and

an I/O signal line formed of a conductive material passing through said via and coupled to ~~said~~ said I/O interconnect structure;

wherein the chip scale package ~~said packaging for the device is formed prior to the formation of any of the plurality of electronic circuits~~ permits said I/O interconnect to be electrically coupled to said top surface through said I/O signal line routed through said via.

23. (As filed) The package of claim 22, further including a plurality of additional I/O interconnects, and wherein all of said I/O interconnects are located within a surface area corresponding to the bottom surface of said body.

24. (Amended) The package of claim 22 wherein the package is adapted such that an ~~said~~ electronic circuit and said I/O interconnects can be formed during a manufacturing process on opposite sides of said semiconductor body.

25. (Amended) The package of claim 22, wherein said package is contained within a single semiconductor wafer including a plurality of additional identical packages for a corresponding plurality of die formed in said single semiconductor wafer.

26. (Amended) The package of claim 22, wherein said via is ~~vias are~~ filled with a conductive material capable of withstanding a high temperature cycle associated with a later manufacturing operation.

27. (As filed) The package of claim 22, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said body.

28. (As filed) The package of claim 22, wherein said I/O interconnect is a bottom side conductive pad located on the bottom side of said body.

29. (As filed) The package of claim 28, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said die, and wherein said top side conductive pad is smaller than said bottom side conductive pad.

30. (As filed) The package of claim 22, wherein said I/O interconnect includes a conductive bump structure.

Please add new claims 49 – 60

49. (New) A semiconductor wafer including an integrated chip scale package to be used for integrated circuits, the wafer comprising:

a top surface and a bottom surface; and

wherein the semiconductor wafer is an unprocessed wafer having no active circuit layers or interconnect layers present on said top surface or said bottom surface of the semiconductor wafer;

a plurality of vias formed in the unprocessed semiconductor wafer, each via having a via top portion beginning at said top surface of the unprocessed semiconductor wafer and extending through to a via bottom portion on said bottom surface of the unprocessed semiconductor wafer;

wherein at least some of said plurality of vias include an input/output (I/O) interconnect structure physically and electrically coupled to said via bottom portion, and said I/O interconnect structure is located within an area on the bottom surface of the unprocessed wafer; and

wherein the I/O interconnect structure is adapted such that an active circuit which is fabricated on the unprocessed semiconductor wafer as part of an integrated circuit at a later time than the I/O interconnect structure can be electrically connected to another integrated circuit without requiring further packaging operations to form pads or bumps for connecting I/O signals of such active circuit to such another integrated circuit.

50. (New) The semiconductor wafer of claim 49, wherein at least some of said plurality of vias are filled with a conductive material capable of withstanding a high temperature cycle associated with a manufacturing operation used later to make said active circuit.

51. (New) The semiconductor wafer of claim 49, wherein at least some of said plurality of vias are filled with an insulating material capable of providing support for the semiconductor wafer during a manufacturing operation used later to make said active circuit.

52. (New) The semiconductor wafer of claim 49 wherein said via is substantially larger than a minimum feature size used in fabricating said active circuit.

53. (New) The semiconductor wafer of claim 52, wherein said via is about 4 mils in diameter.

54. (New) The semiconductor wafer of claim 49, further including a passivation layer formed on at least said top surface.

55. (New) The semiconductor wafer of claim 49, wherein the input/output (I/O) interconnect structure includes a plurality of solder bumps and/or pads.

56. (New) The semiconductor wafer of claim 49, wherein the semiconductor wafer includes a plurality of chip-scale packages.

57. (New) The semiconductor wafer of claim 55, further including a plurality of integrated circuits on the semiconductor wafer coupled to said plurality of chip-scale packages.

58. (New) The semiconductor wafer of claim 55, wherein said plurality of integrated circuits on the semiconductor wafer are memory devices.

59. (New) The semiconductor wafer of claim 55, further including a second I/O structure on a top surface of the semiconductor wafer.

60. (New) The semiconductor wafer of claim 55, wherein said bottom portion for at least some of said plurality of vias is substantially larger than a corresponding top portion.